IEEE CASS Talks 2019

IEEE CASS Rio Grande do Sul Chapter

Porto Alegre, Brasil

IEEE CIRCUITS AND SYSTEMS SOCIETY

Instituto de Informática, UFRGS, Auditório INFERIOR, prédio 43413

15:30, April 30, 2019

Prof. Leonel Sousa, INESC-ID, Portugal
Distingued Lecturer IEEE CASS

Modeling Performance and Energy-Efficiency of Multi-Cores: The Cache-Aware Roofline Approach and The Intel Advisor

Abstract

As architectures evolve towards more complex multi-core designs, deciding what optimizations provide the best trade-off between performance and efficiency is becoming a prominent issue. To help in this decision process, a set of fundamental Cache-aware Roofline Models (CARMs) are presented in this tutorial, which allow characterizing the upper bounds of contemporary parallel architectures for performance, power, energy and energy-efficiency (i.e., multi-core CPU and GPU architectures). These models evaluate how key micro- architectural aspects, such as accessing different functional units or different memory hierarchy levels, affect the attainable performance, power and energy-efficiency.

Recently, the performance CARM was integrated by Intel as a fully supported feature into their proprietary Intel Advisor software tool, and it is described as "an incredibly useful diagnosis tool (...) that developers can use to guide them (in the application optimization process), ensuring that they can squeeze the maximum performance out of their code with minimal time and effort". The proposed models are also rigorously validated on different CPU and GPU architectures by relying on hardware counters and specifically developed performance/power monitoring tools. Experimental results show a very high accuracy of the proposed models, and their ability to provide more intuitive and useful guidelines than the state-of-the-art approaches, when characterizing real-world applications from standard benchmark suites.

Short Bio

Leonel Sousa is currently Full Professor and Chair of the Electrical and Computer Engineering Department at the IST, Universidade de Lisboa and a Senior Researcher with the INESC-ID in Portugal. He has been vising professor in several universities abroad, he spent a few months in Japan with a prestigious JSPS Invitation Fellowship for Research and he has been at the Carnegie Mellon University. His research interests include high performance computing, computer architectures, computer arithmetic and multimedia systems. He has given more than 30 keynotes, invited talks and tutorials, he has authored or co-authored more than 250 papers appearing in international journals and conferences and edited five special issues of international journals. He served in the organization of several international conferences and he is currently an Associate Editor of the IEEE Transactions on Computers, IEEE Transactions on Multimedia and IEEE Transactions on Circuits and Systems for Video Technology. He is member of the IFIP WG10.3 on concurrent systems, Fellow of the IET and Distinguished Scientist of the ACM.

IEEE CAS IEEE CIRCUITS AND SYSTEMS SOCIETY UFRGS UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL UFRGS PGMICRO .inf INSTITUTO DE INFORMÁTICA UFRGS